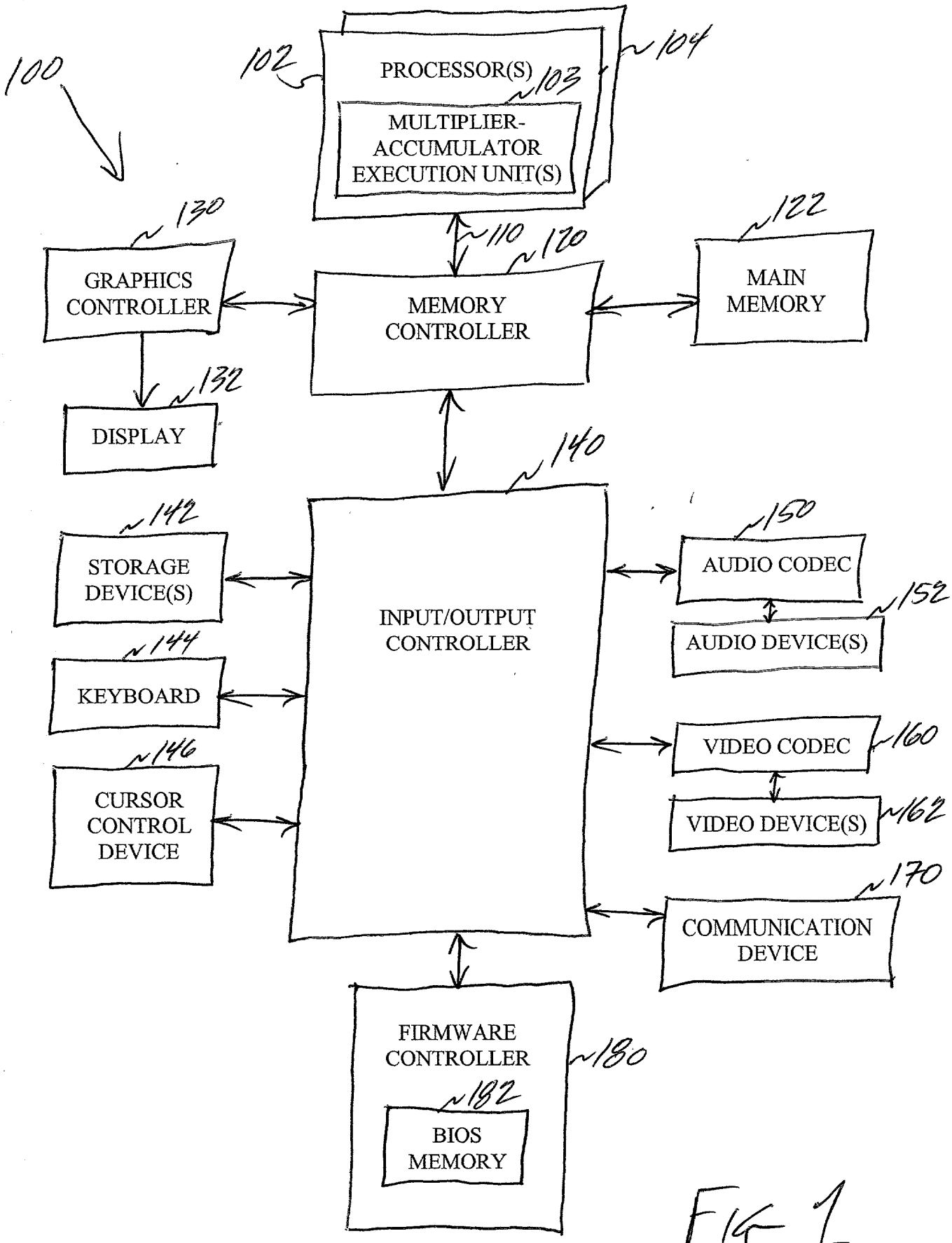
100
102
PROCESSOR(S)
103
MULTIPLIER-ACCUMULATOR EXECUTION UNIT(S)
104
110
120
MEMORY CONTROLLER
122
MAIN MEMORY
130
GRAPHICS CONTROLLER
132
DISPLAY
140
INPUT/OUTPUT CONTROLLER
142
STORAGE DEVICE(S)
144
KEYBOARD
146
CURSOR CONTROL DEVICE
150
AUDIO CODEC
152
AUDIO DEVICE(S)
160
VIDEO CODEC
162
VIDEO DEVICE(S)
170
COMMUNICATION DEVICE
180
FIRMWARE CONTROLLER
182
BIOS MEMORY

FIG. 1

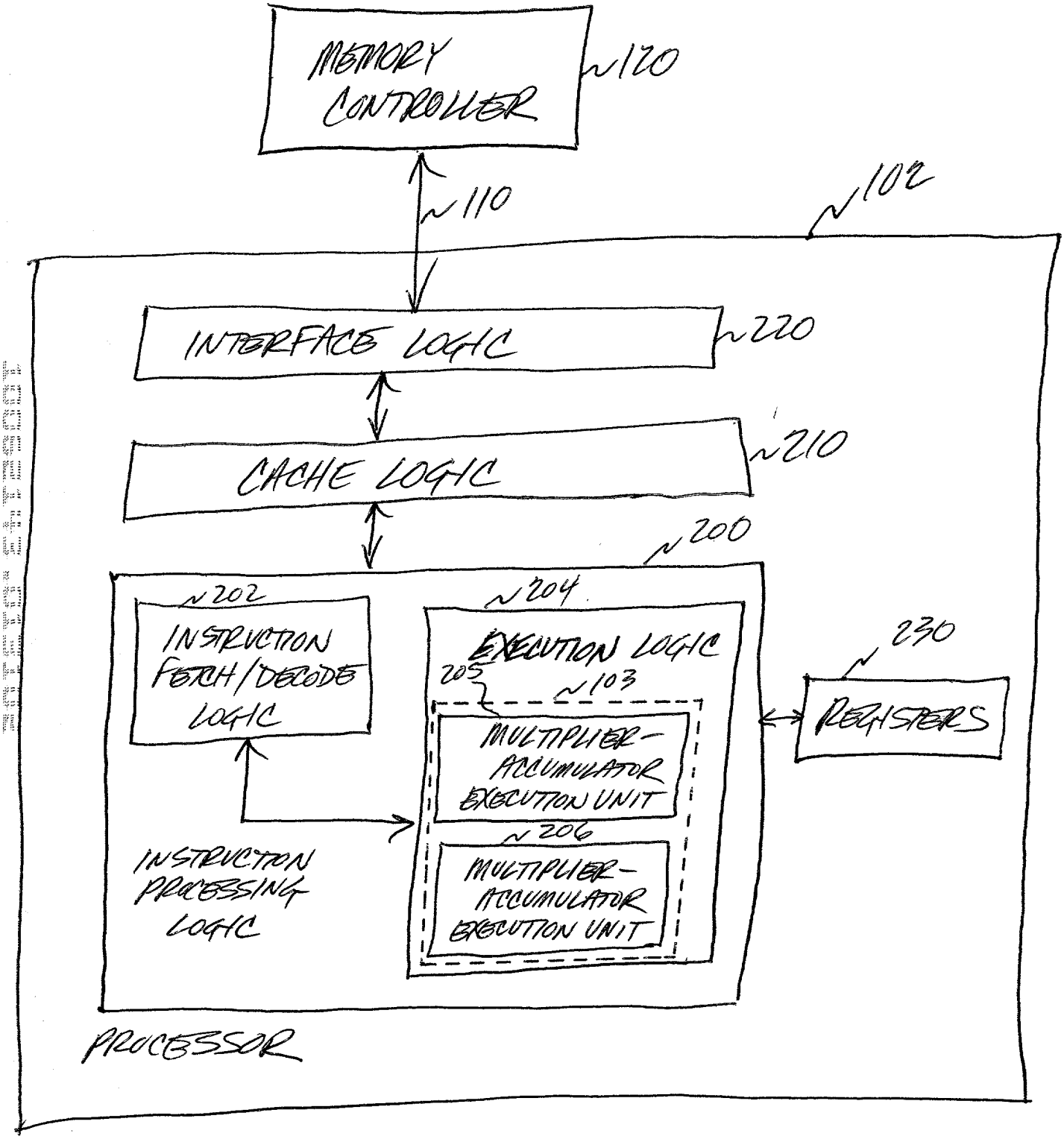
MEMORY CONTROLLER
120
110
102
INTERFACE LOGIC
220
CACHE LOGIC
210
200
202
INSTRUCTION FETCH/DECODE LOGIC
204
EXECUTION LOGIC
205
103
MULTIPLIER-ACCUMULATOR EXECUTION UNIT
206
MULTIPLIER-ACCUMULATOR EXECUTION UNIT
230
REGISTERS
INSTRUCTION PROCESSING LOGIC
PROCESSOR

FIG. 2

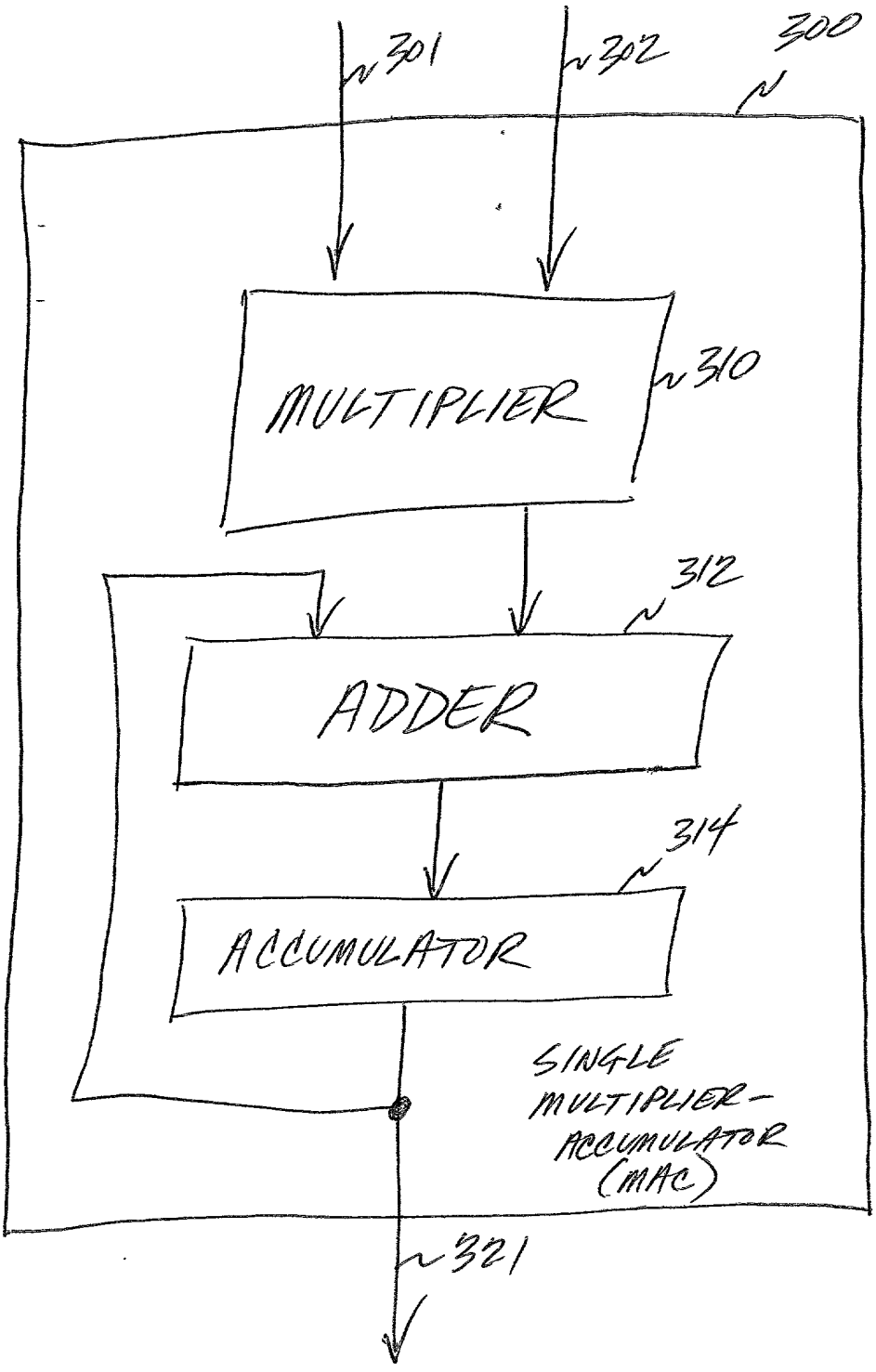
301
302
300
MULTIPLIER
310
312
ADDER
314
ACCUMULATOR
SINGLE MULTIPLIER-ACCUMULATOR (MAC)
321

FIG. 3

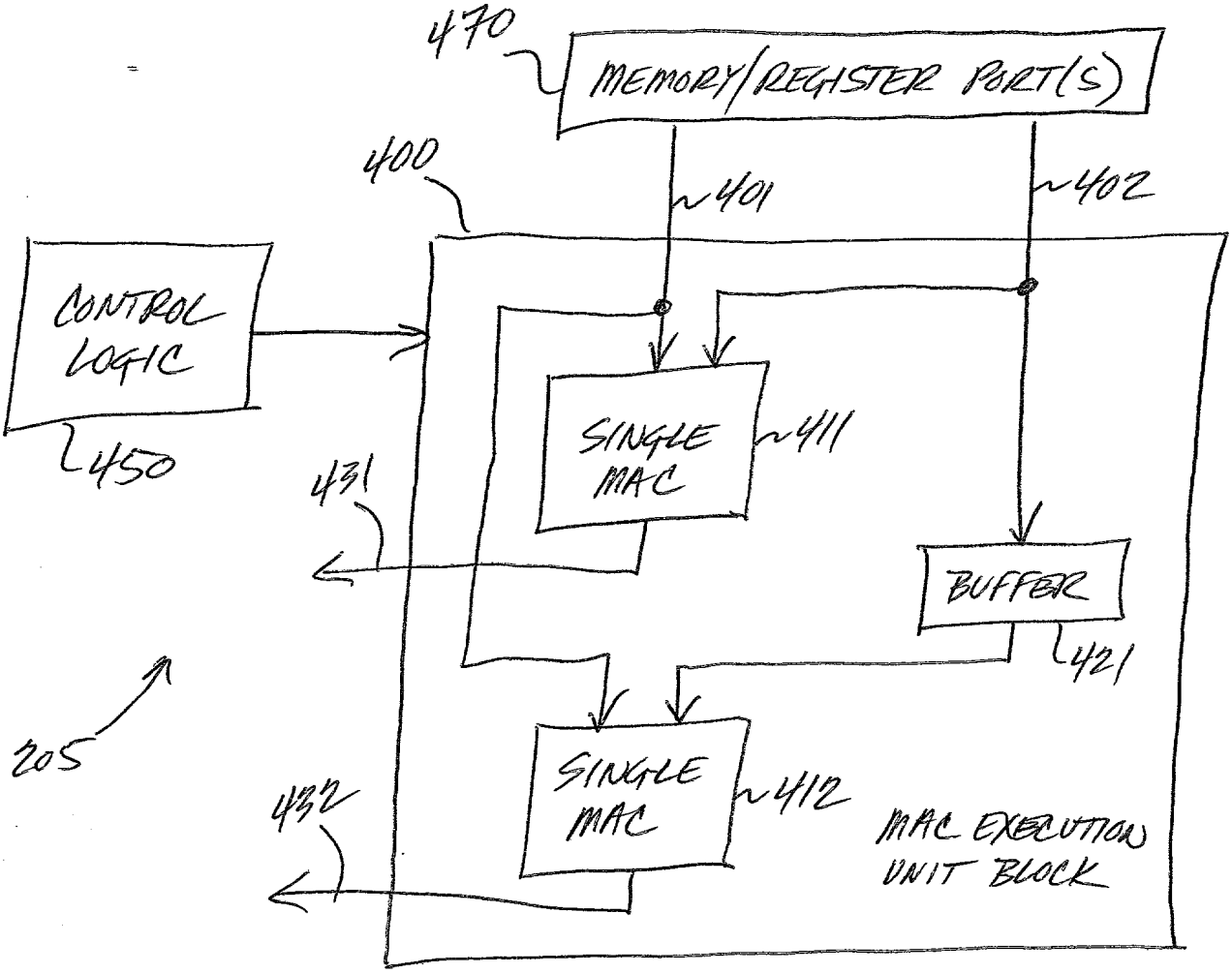
470
MEMORY/REGISTER PORT(S)
400
401
402
CONTROL LOGIC
450
SINGLE MAC
411
431
BUFFER
421
205
SINGLE MAC
412
432
MAC EXECUTION UNIT BLOCK

FIG. 4

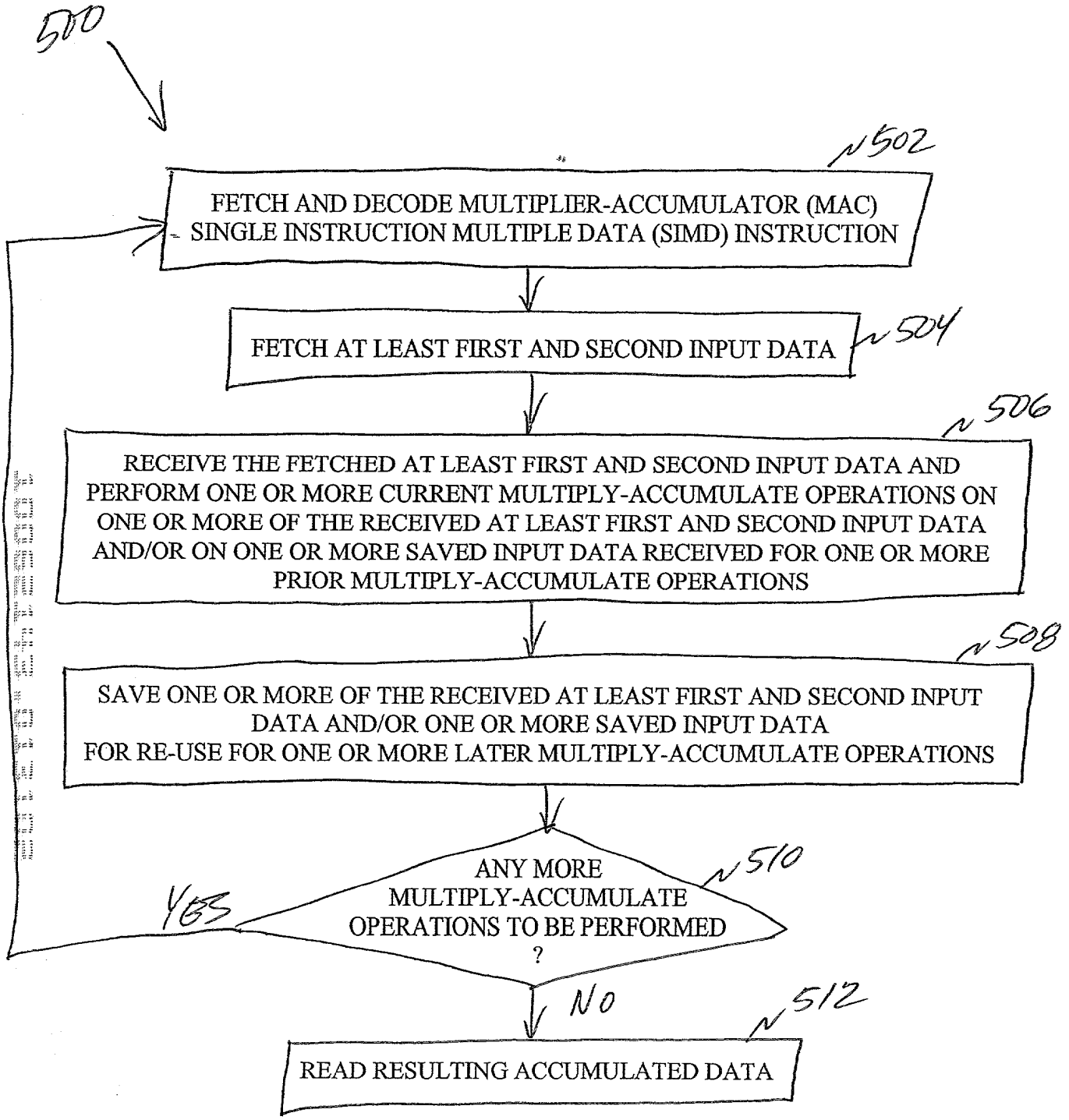
500
502
FETCH AND DECODE MULTIPLIER-ACCUMULATOR (MAC) SINGLE INSTRUCTION MULTIPLE DATA (SIMD) INSTRUCTION
504
FETCH AT LEAST FIRST AND SECOND INPUT DATA
506
RECEIVE THE FETCHED AT LEAST FIRST AND SECOND INPUT DATA AND PERFORM ONE OR MORE CURRENT MULTIPLY-ACCUMULATE OPERATIONS ON ONE OR MORE OF THE RECEIVED AT LEAST FIRST AND SECOND INPUT DATA AND/OR ON ONE OR MORE SAVED INPUT DATA RECEIVED FOR ONE OR MORE PRIOR MULTIPLY-ACCUMULATE OPERATIONS
508
SAVE ONE OR MORE OF THE RECEIVED AT LEAST FIRST AND SECOND INPUT DATA AND/OR ONE OR MORE SAVED INPUT DATA FOR RE-USE FOR ONE OR MORE LATER MULTIPLY-ACCUMULATE OPERATIONS
510
ANY MORE MULTIPLY-ACCUMULATE OPERATIONS TO BE PERFORMED ?
YES
NO
512
READ RESULTING ACCUMULATED DATA

FIG. 5

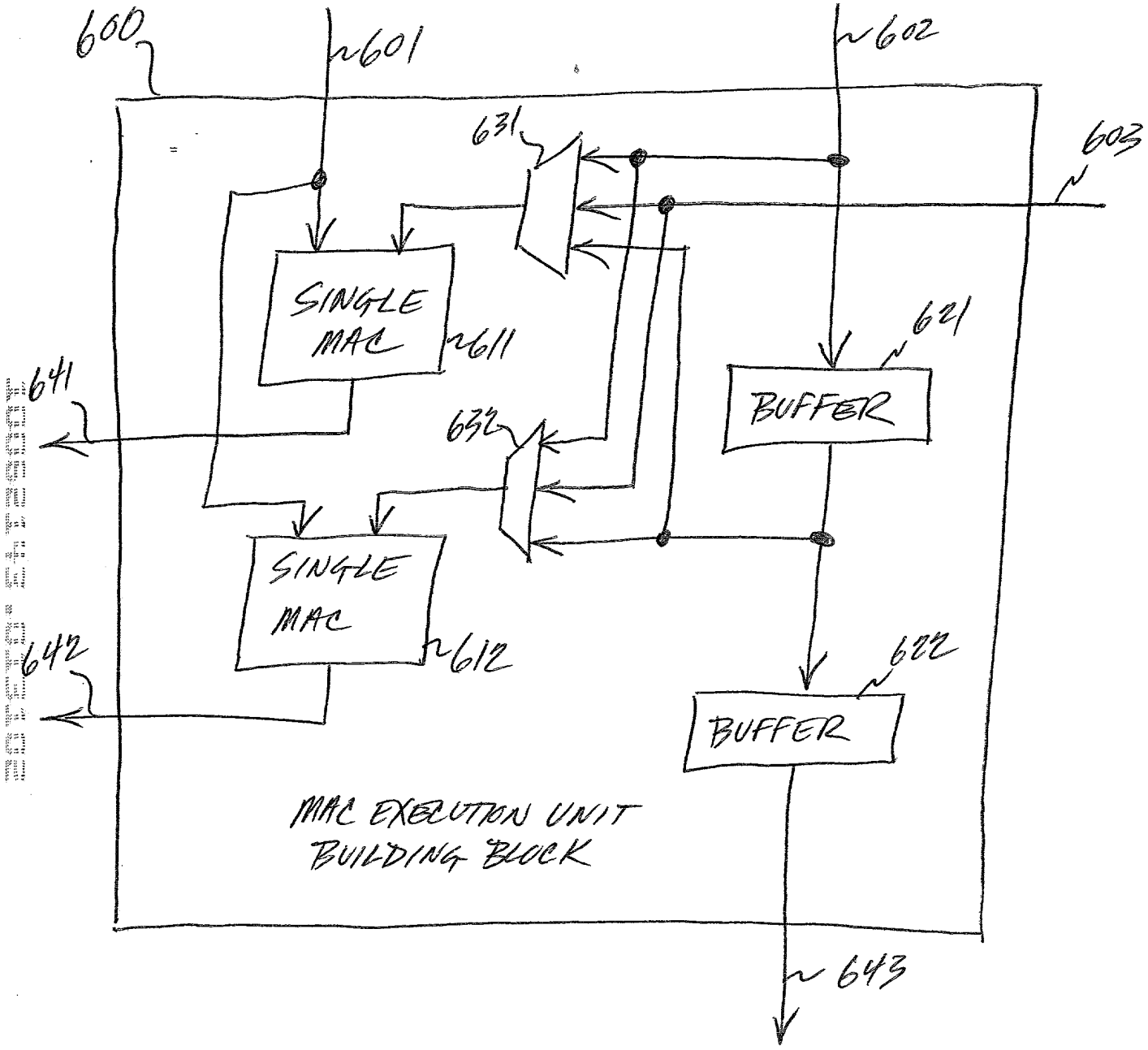
600
601
602
603
631
SINGLE MAC
611
621
BUFFER
641
632
SINGLE MAC
612
642
622
BUFFER
MAC EXECUTION UNIT BUILDING BLOCK
643

FIG. 6

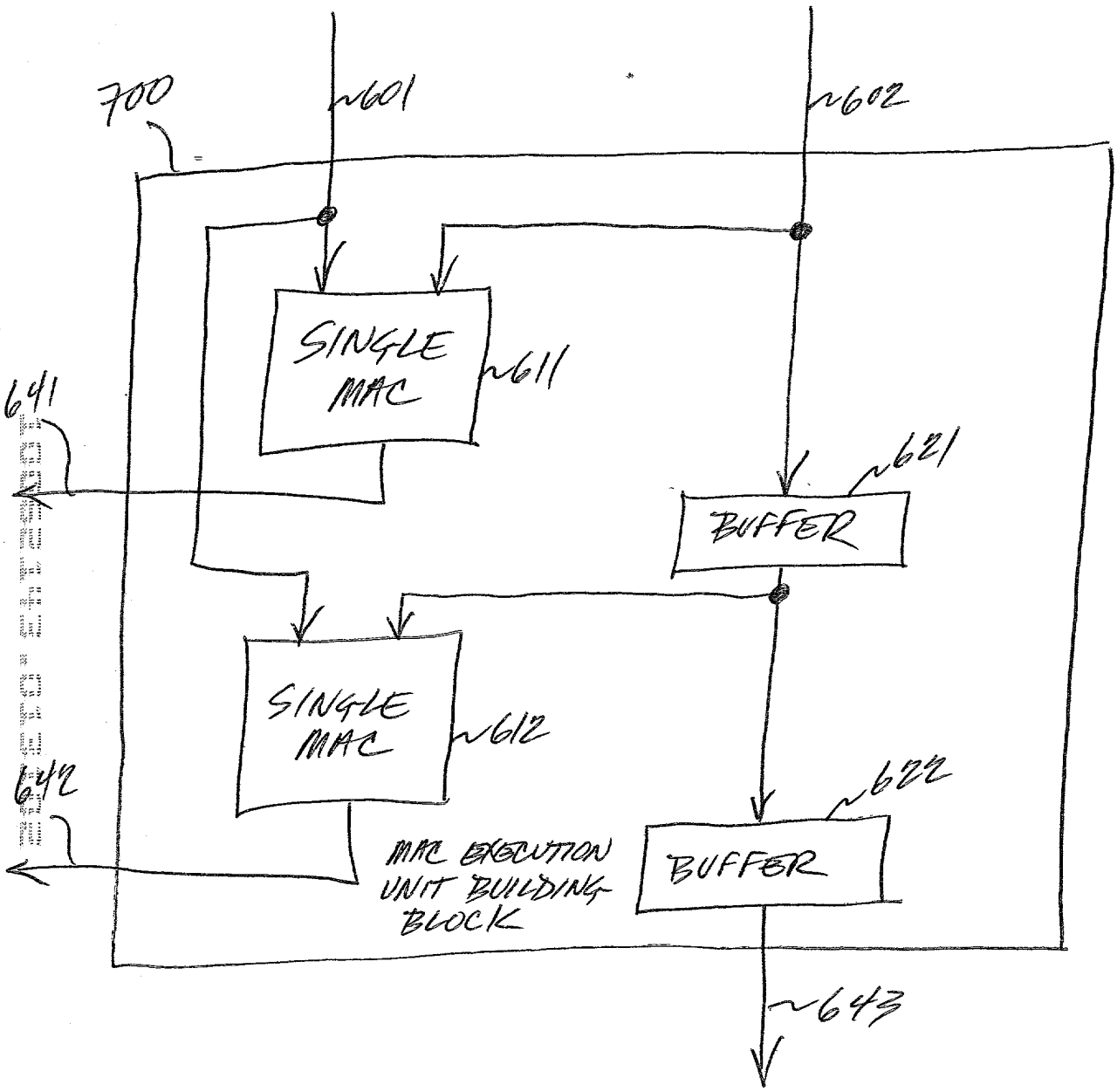
700
601
602
SINGLE MAC
611
641
621
BUFFER
SINGLE MAC
612
642
622
MAC EXECUTION UNIT BUILDING BLOCK
BUFFER
643

FIG. 7

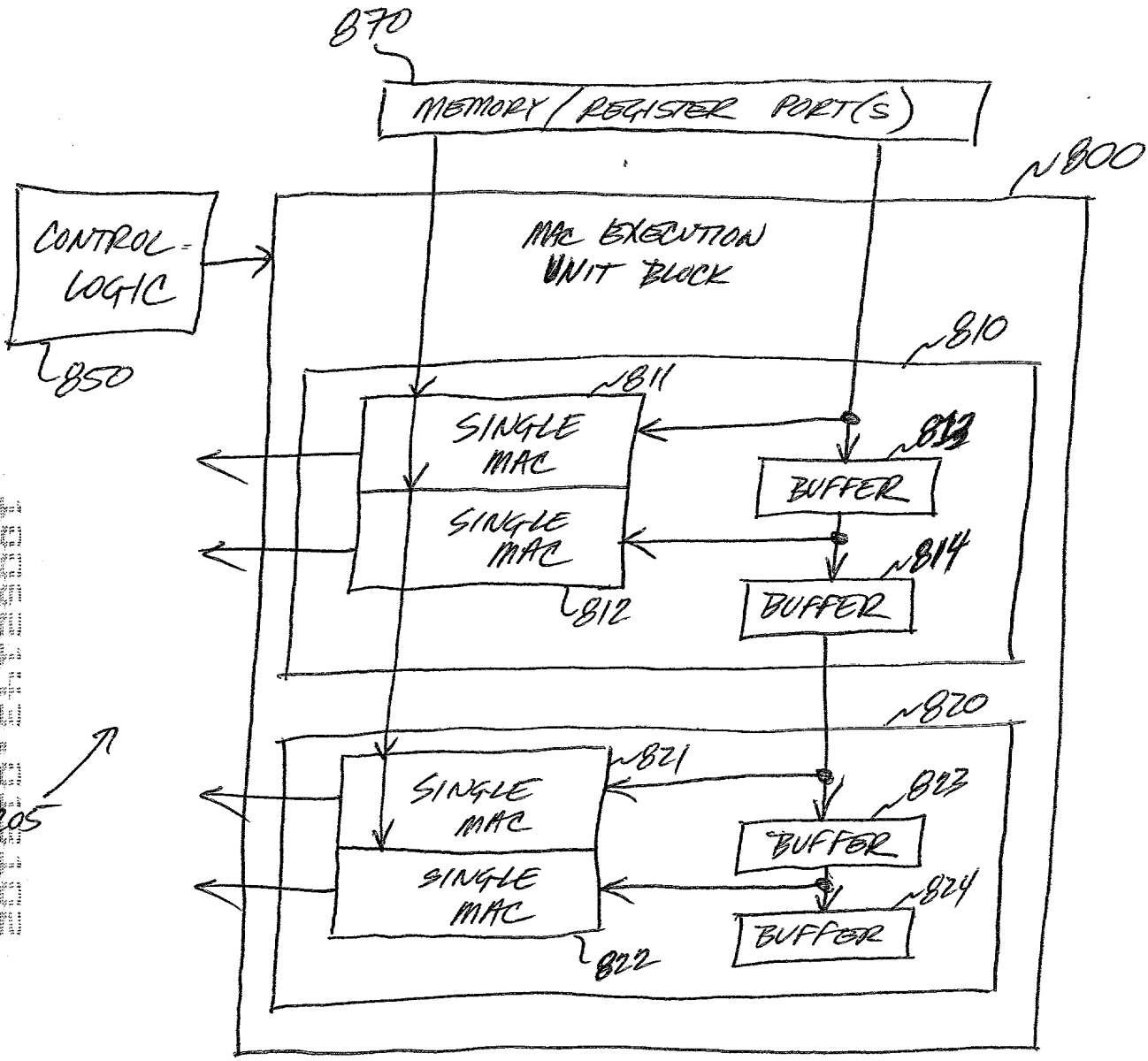
870
MEMORY / REGISTER PORT(S)
800
CONTROL LOGIC
850
MAC EXECUTION UNIT BLOCK
810
811
SINGLE MAC
SINGLE MAC
812
813
BUFFER
814
BUFFER
870
821
SINGLE MAC
SINGLE MAC
822
823
BUFFER
824
BUFFER
205

FIG. 8

900

MAC	Computation Cycle N		Computation Cycle N+1		Computation Cycle N+2	
	1st MAC Input	2nd MAC Input	1st MAC Input	2nd MAC Input	1st MAC Input	2nd MAC Input
811: y(3)	c(31)	x(-28)	c(30)	x(-27)	c(29)	x(-26)
812: y(2)	c(31)	x(-29)	c(30)	x(-28)	c(29)	x(-27)
821: y(1)	c(31)	x(-30)	c(30)	x(-29)	c(29)	x(-28)
822: y(0)	c(31)	x(-31)	c(30)	x(-30)	c(29)	x(-29)

FIG. 9

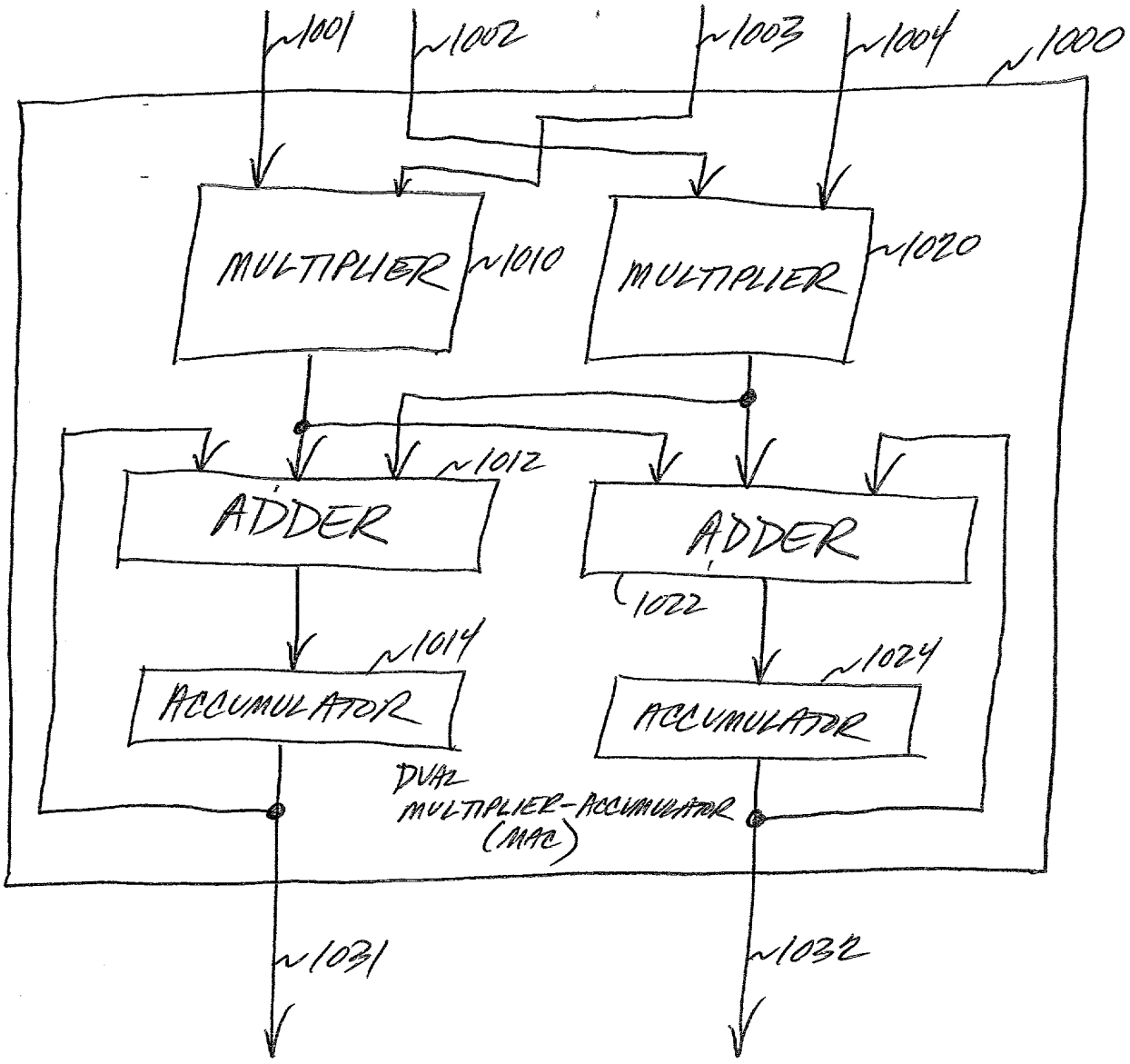
1001
1002
1003
1004
1000
MULTIPLIER
1010
MULTIPLIER
1020
ADDER
1012
ADDER
1022
1014
ACCUMULATOR
1024
ACCUMULATOR
DUAL
MULTIPLIER-ACCUMULATOR
(MAC)
1031
1032

FIG. 10

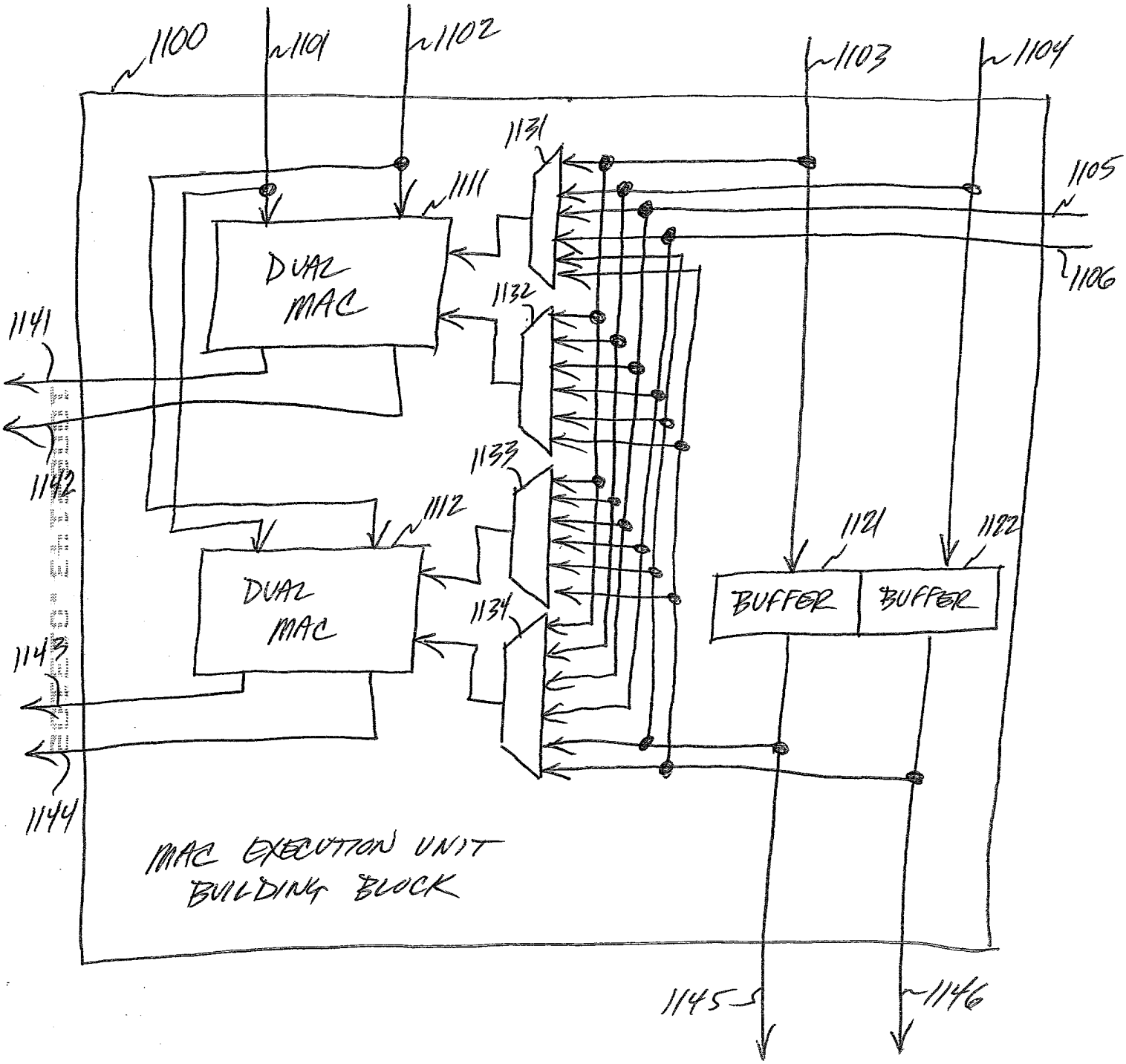
1100
1101
1102
1103
1104
1105
1106
1111
1112
1121
1122
1131
1132
1133
1134
1141
1142
1143
1144
1145
1146
DUAL MAC
DUAL MAC
BUFFER
BUFFER
MAC EXECUTION UNIT BUILDING BLOCK

FIG. 11

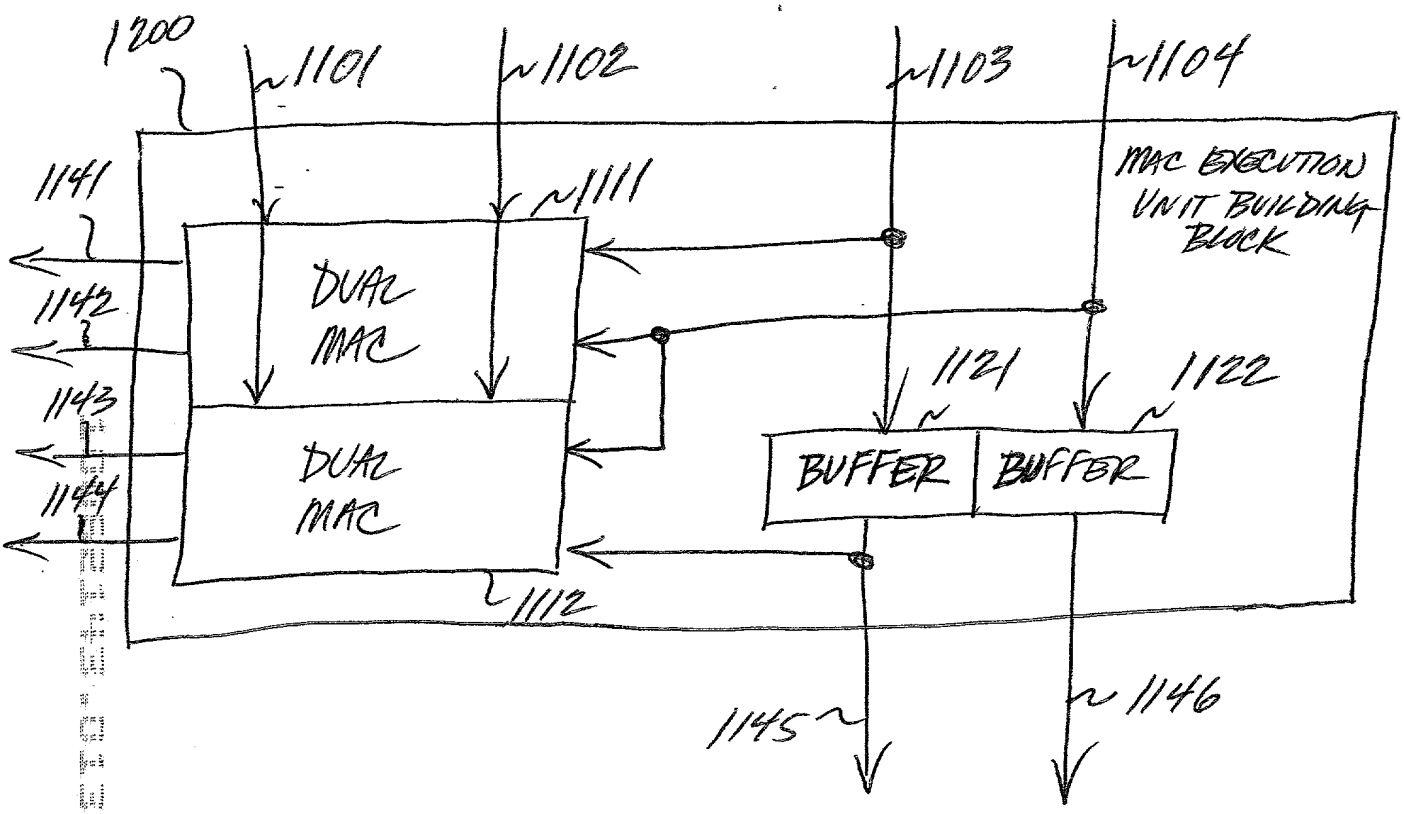
1200
1101
1102
1103
1104
MAC EXECUTION UNIT BUILDING BLOCK
1141
1111
1142
DUAL MAC
1143
1121
1122
DUAL MAC
BUFFER
BUFFER
1144
1112
1145
1146

FIG. 12

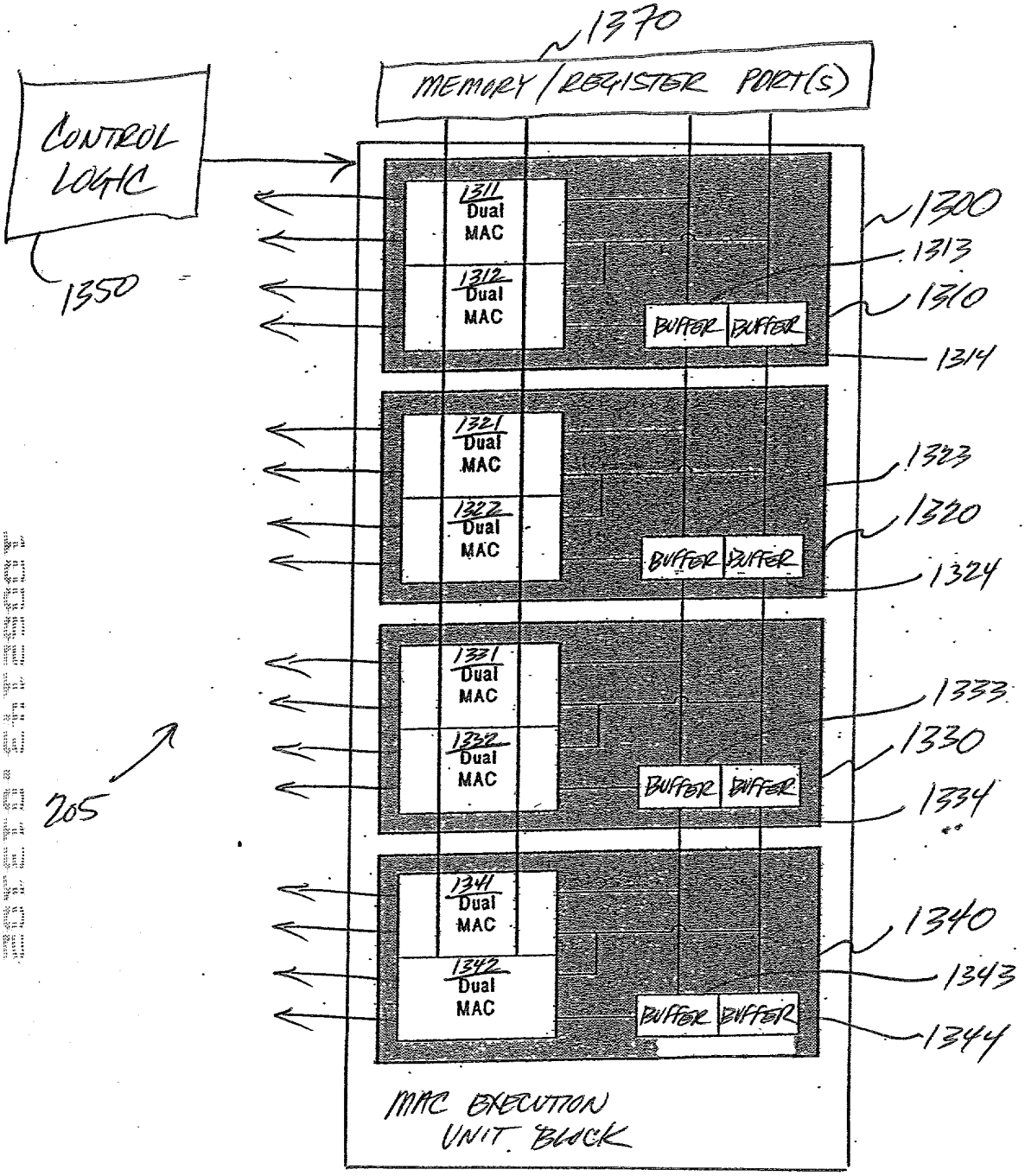
1370
MEMORY / REGISTER PORT(S)
CONTROL LOGIC
1350
1311 Dual MAC
1312 Dual MAC
1300
1313
1310
BUFFER
BUFFER
1314
1321 Dual MAC
1322 Dual MAC
1323
1320
BUFFER
BUFFER
1324
1331 Dual MAC
1332 Dual MAC
1333
1330
BUFFER
BUFFER
1334
1341 Dual MAC
1342 Dual MAC
1340
1343
BUFFER
BUFFER
1344
MAC EXECUTION UNIT BLOCK
205

FIG. 13

1400

MAC	Computation Cycle N				Computation Cycle N+1				Computation Cycle N+2			
	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
1311: y(7)	c(30)	x(-23)	c(31)	x(-24)	c(28)	x(-21)	c(29)	x(-22)	c(26)	x(-19)	c(27)	x(-20)
1312: y(6)	c(30)	x(-24)	c(31)	x(-25)	c(28)	x(-22)	c(29)	x(-23)	c(26)	x(-20)	c(27)	x(-21)
1321: y(5)	c(30)	x(-25)	c(31)	x(-26)	c(28)	x(-23)	c(29)	x(-24)	c(26)	x(-21)	c(27)	x(-22)
1322: y(4)	c(30)	x(-26)	c(31)	x(-27)	c(28)	x(-24)	c(29)	x(-25)	c(26)	x(-22)	c(27)	x(-23)
1331: y(3)	c(30)	x(-27)	c(31)	x(-28)	c(28)	x(-25)	c(29)	x(-26)	c(26)	x(-23)	c(27)	x(-24)
1332: y(2)	c(30)	x(-28)	c(31)	x(-29)	c(28)	x(-26)	c(29)	x(-27)	c(26)	x(-24)	c(27)	x(-25)
1341: y(1)	c(30)	x(-29)	c(31)	x(-30)	c(28)	x(-27)	c(29)	x(-28)	c(26)	x(-25)	c(27)	x(-26)
1342: y(0)	c(30)	x(-30)	c(31)	x(-31)	c(28)	x(-28)	c(29)	x(-29)	c(26)	x(-26)	c(27)	x(-27)

FIG. 14

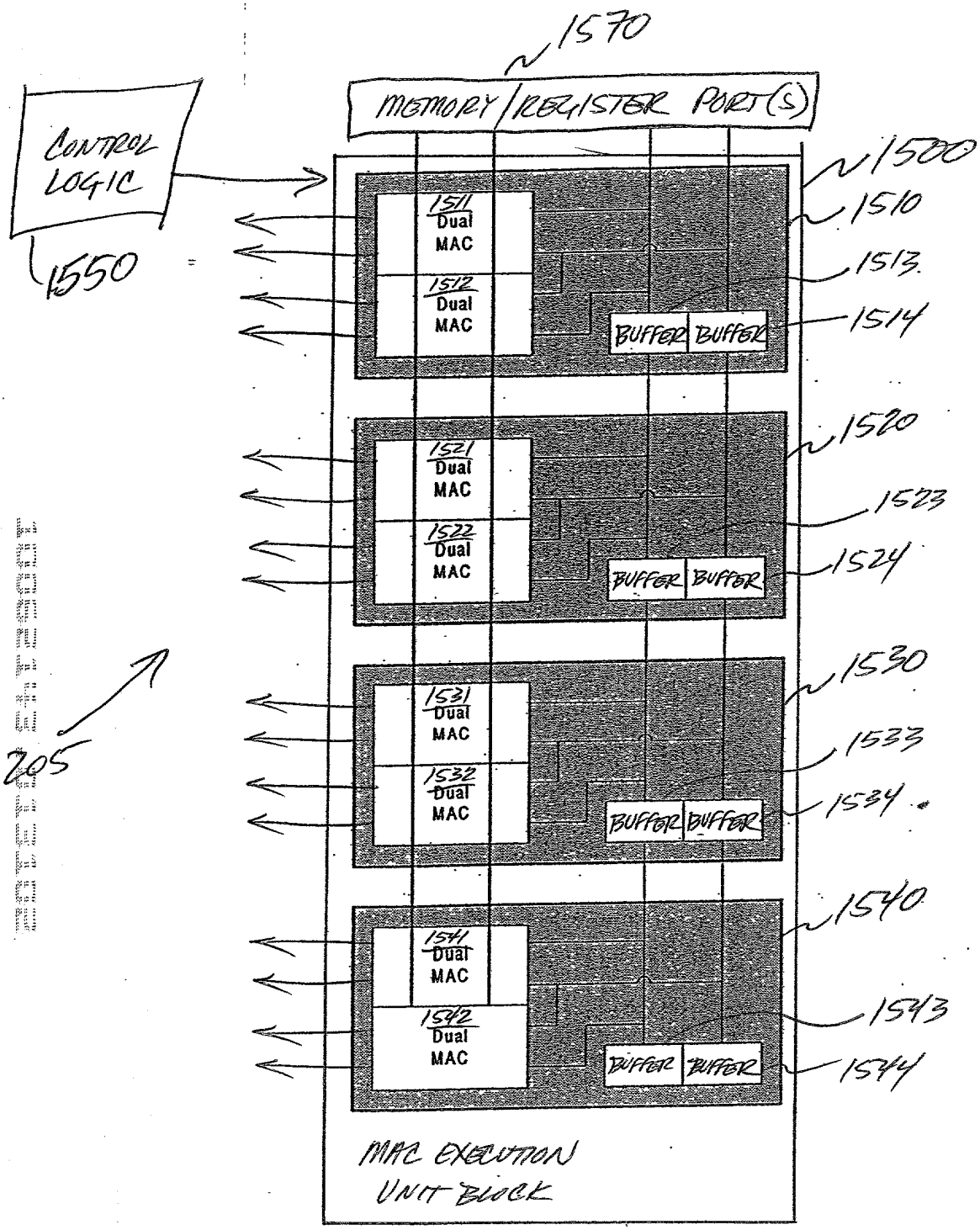
1570
MEMORY/REGISTER PORT(S)
CONTROL LOGIC
1550
1500
1510
1511 Dual MAC
1512 Dual MAC
1513
1514
BUFFER
BUFFER
1520
1521 Dual MAC
1522 Dual MAC
1523
1524
BUFFER
BUFFER
1530
1531 Dual MAC
1532 Dual MAC
1533
1534
BUFFER
BUFFER
1540
1541 Dual MAC
1542 Dual MAC
1543
1544
BUFFER
BUFFER
MAC EXECUTION UNIT BLOCK
205

FIG. 15

1600

MAC	Computation Cycle N				Computation Cycle N+1				Computation Cycle N+2			
	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
1511: $y(3)_r$	$c(31)_r$	$x(-28)_r$	$c(31)_i$	$x(-28)_i$	$c(30)_r$	$x(-27)_r$	$c(30)_i$	$x(-27)_i$	$c(29)_r$	$x(-26)_r$	$c(29)_i$	$x(-26)_i$
1512: $y(3)_i$	$c(31)_r$	$x(-28)_i$	$c(31)_i$	$x(-28)_r$	$c(30)_r$	$x(-27)_i$	$c(30)_i$	$x(-27)_r$	$c(29)_r$	$x(-26)_i$	$c(29)_i$	$x(-26)_r$
1521: $y(2)_r$	$c(31)_r$	$x(-29)_r$	$c(31)_i$	$x(-29)_i$	$c(30)_r$	$x(-28)_r$	$c(30)_i$	$x(-28)_i$	$c(29)_r$	$x(-27)_r$	$c(29)_i$	$x(-27)_i$
1522: $y(2)_i$	$c(31)_r$	$x(-29)_i$	$c(31)_i$	$x(-29)_r$	$c(30)_r$	$x(-28)_i$	$c(30)_i$	$x(-28)_r$	$c(29)_r$	$x(-27)_i$	$c(29)_i$	$x(-27)_r$
1531: $y(1)_r$	$c(31)_r$	$x(-30)_r$	$c(31)_i$	$x(-30)_i$	$c(30)_r$	$x(-29)_r$	$c(30)_i$	$x(-29)_i$	$c(29)_r$	$x(-28)_r$	$c(29)_i$	$x(-28)_i$
1532: $y(1)_i$	$c(31)_r$	$x(-30)_i$	$c(31)_i$	$x(-30)_r$	$c(30)_r$	$x(-29)_i$	$c(30)_i$	$x(-29)_r$	$c(29)_r$	$x(-28)_i$	$c(29)_i$	$x(-28)_r$
1541: $y(0)_r$	$c(31)_r$	$x(-31)_r$	$c(31)_i$	$x(-31)_i$	$c(30)_r$	$x(-30)_r$	$c(30)_i$	$x(-30)_i$	$c(29)_r$	$x(-29)_r$	$c(29)_i$	$x(-29)_i$
1542: $y(0)_i$	$c(31)_r$	$x(-31)_i$	$c(31)_i$	$x(-31)_r$	$c(30)_r$	$x(-30)_i$	$c(30)_i$	$x(-30)_r$	$c(29)_r$	$x(-29)_i$	$c(29)_i$	$x(-29)_r$

FIG. 16

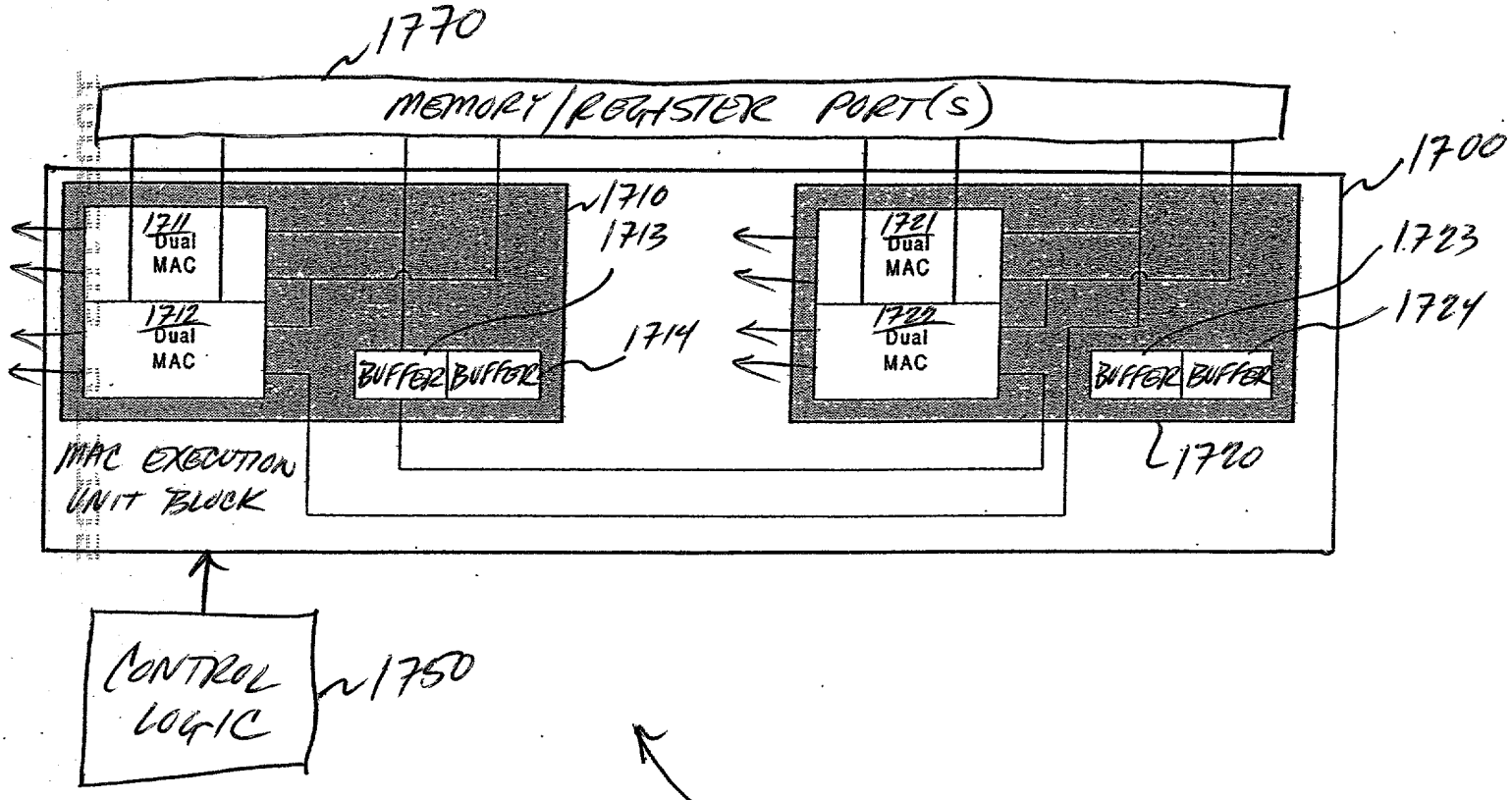
1770
MEMORY/REGISTER PORT(S)
1700
1710
1711
Dual MAC
1712
Dual MAC
1713
1714
BUFFER
BUFFER
1721
Dual MAC
1722
Dual MAC
1723
1724
BUFFER
BUFFER
1720
MAC EXECUTION UNIT BLOCK
CONTROL LOGIC
1750
205

FIG. 17

1800

Computation Cycle N									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
1711: y(1)	c(28)	x(-27)	c(29)	x(-28)	1721: y(1)	c(30)	x(-29)	c(31)	x(-30)
1712: y(0)	c(28)	x(-28)	c(29)	x(-29)	1722: y(0)	c(30)	x(-30)	c(31)	x(-31)
Computation Cycle N+1									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
1711: y(1)	c(24)	x(-23)	c(25)	x(-24)	1721: y(1)	c(26)	x(-25)	c(27)	x(-26)
1712: y(0)	c(24)	x(-24)	c(25)	x(-25)	1722: y(0)	c(26)	x(-26)	c(27)	x(-27)
Computation Cycle N+2									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
1711: y(1)	c(20)	x(-19)	c(21)	x(-20)	1721: y(1)	c(22)	x(-21)	c(23)	x(-22)
1712: y(0)	c(20)	x(-20)	c(21)	x(-21)	1722: y(0)	c(22)	x(-22)	c(23)	x(-23)

Fig. 18

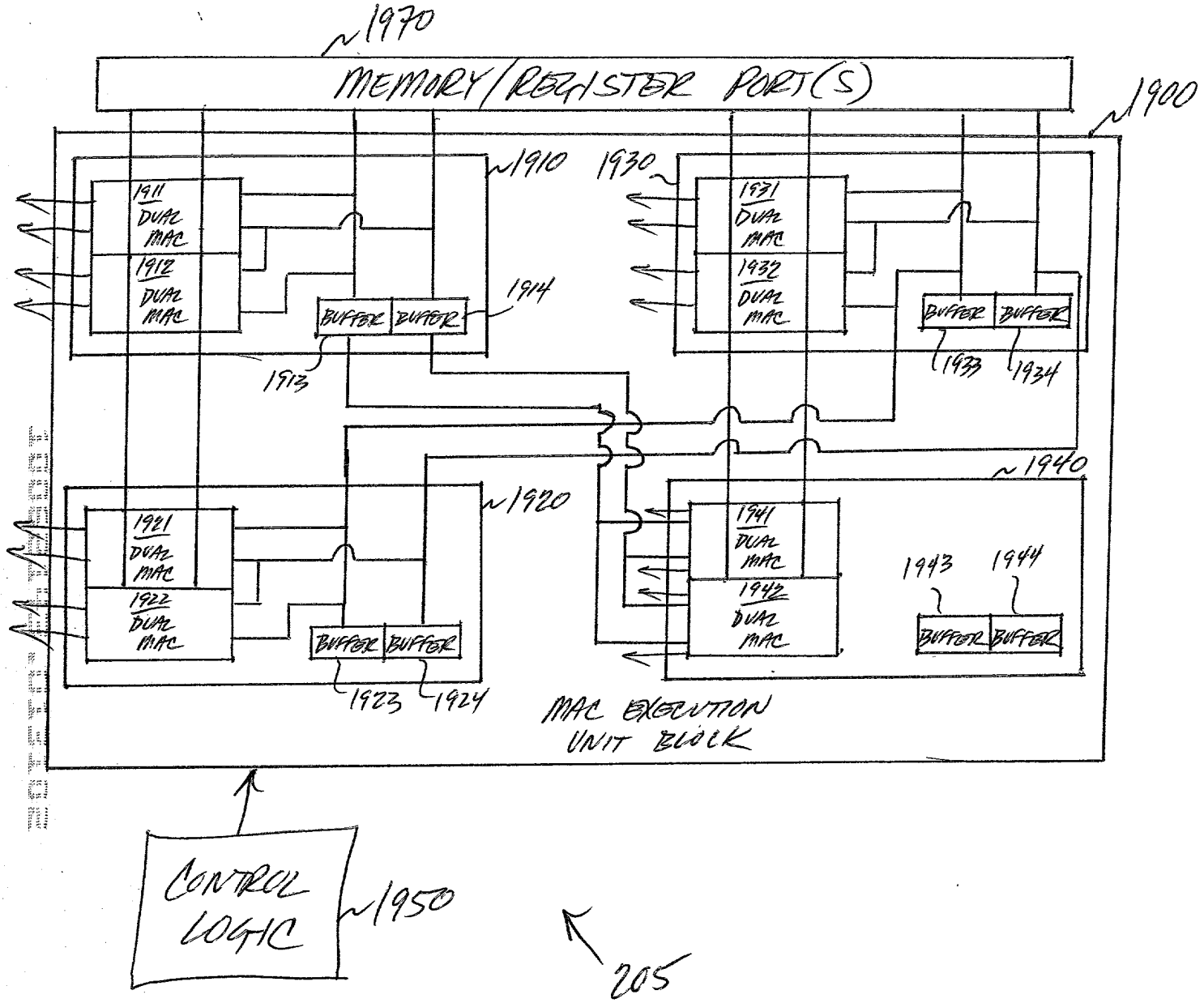
1970
MEMORY/REGISTER PORT(S)
1900
1910
1911 DUAL MAC
1912 DUAL MAC
BUFFER
BUFFER
1914
1913
1930
1931 DUAL MAC
1932 DUAL MAC
BUFFER
BUFFER
1933
1934
1940
1920
1921 DUAL MAC
1922 DUAL MAC
BUFFER
BUFFER
1923
1924
1941 DUAL MAC
1942 DUAL MAC
1943
1944
BUFFER
BUFFER
MAC EXECUTION UNIT BLOCK
CONTROL LOGIC
1950
205

FIG. 19

2000.

Computation Cycle N									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
1911: $y(1)_r$	$c(30)_r$	$x(-29)_r$	$c(30)_i$	$x(-29)_i$	1931: $y(1)_r$	$c(31)_r$	$x(-30)_r$	$c(31)_i$	$x(-30)_i$
1912: $y(1)_i$	$c(30)_r$	$x(-29)_i$	$c(30)_i$	$x(-29)_r$	1932: $y(1)_i$	$c(31)_r$	$x(-30)_i$	$c(31)_i$	$x(-30)_r$
1921: $y(0)_r$	$c(30)_r$	$x(-30)_r$	$c(30)_i$	$x(-30)_i$	1941: $y(0)_r$	$c(31)_r$	$x(-31)_r$	$c(31)_i$	$x(-31)_i$
1922: $y(0)_i$	$c(30)_r$	$x(-30)_i$	$c(30)_i$	$x(-30)_r$	1942: $y(0)_i$	$c(31)_r$	$x(-31)_i$	$c(31)_i$	$x(-31)_r$
Computation Cycle N+1									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
1911: $y(1)_r$	$c(28)_r$	$x(-27)_r$	$c(28)_i$	$x(-27)_i$	1931: $y(1)_r$	$c(29)_r$	$x(-28)_r$	$c(29)_i$	$x(-28)_i$
1912: $y(1)_i$	$c(28)_r$	$x(-27)_i$	$c(28)_i$	$x(-27)_r$	1932: $y(1)_i$	$c(29)_r$	$x(-28)_i$	$c(29)_i$	$x(-28)_r$
1921: $y(0)_r$	$c(28)_r$	$x(-28)_r$	$c(28)_i$	$x(-28)_i$	1941: $y(0)_r$	$c(29)_r$	$x(-29)_r$	$c(29)_i$	$x(-29)_i$
1922: $y(0)_i$	$c(28)_r$	$x(-28)_i$	$c(28)_i$	$x(-28)_r$	1942: $y(0)_i$	$c(29)_r$	$x(-29)_i$	$c(29)_i$	$x(-29)_r$
Computation Cycle N+2									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
1911: $y(1)_r$	$c(26)_r$	$x(-25)_r$	$c(26)_i$	$x(-25)_i$	1931: $y(1)_r$	$c(27)_r$	$x(-26)_r$	$c(27)_i$	$x(-26)_i$
1912: $y(1)_i$	$c(26)_r$	$x(-25)_i$	$c(26)_i$	$x(-25)_r$	1932: $y(1)_i$	$c(27)_r$	$x(-26)_i$	$c(27)_i$	$x(-26)_r$
1921: $y(0)_r$	$c(26)_r$	$x(-26)_r$	$c(26)_i$	$x(-26)_i$	1941: $y(0)_r$	$c(27)_r$	$x(-27)_r$	$c(27)_i$	$x(-27)_i$
1922: $y(0)_i$	$c(26)_r$	$x(-26)_i$	$c(26)_i$	$x(-26)_r$	1942: $y(0)_i$	$c(27)_r$	$x(-27)_i$	$c(27)_i$	$x(-27)_r$

Fig. 20

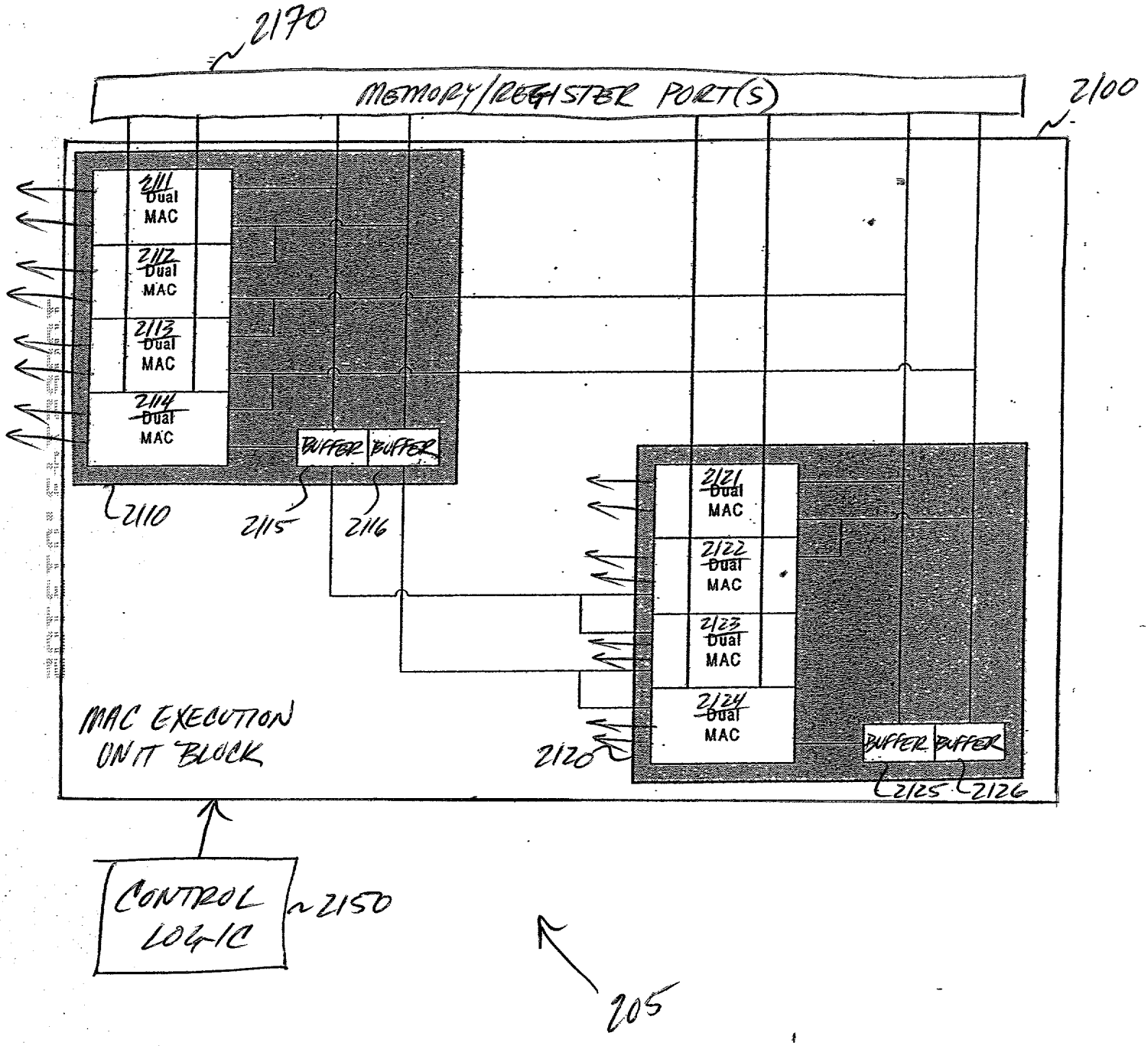
2170
MEMORY/REGISTER PORT(S)
2100
2111 Dual MAC
2112 Dual MAC
2113 Dual MAC
2114 Dual MAC
BUFFER
BUFFER
2110
2115
2116
2121 Dual MAC
2122 Dual MAC
2123 Dual MAC
2124 Dual MAC
BUFFER
BUFFER
2120
2125
2126
MAC EXECUTION UNIT BLOCK
CONTROL LOGIC
2150
205

FIG. 21

2200

Computation Cycle N									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2111: y(3)	c(28)	x(-25)	c(29)	x(-26)	2121: y(3)	c(30)	x(-27)	c(31)	x(-28)
2112: y(2)	c(28)	x(-26)	c(29)	x(-27)	2122: y(2)	c(30)	x(-28)	c(31)	x(-29)
2113: y(1)	c(28)	x(-27)	c(29)	x(-28)	2123: y(1)	c(30)	x(-29)	c(31)	x(-30)
2114: y(0)	c(28)	x(-28)	c(29)	x(-29)	2124: y(0)	c(30)	x(-30)	c(31)	x(-31)
Computation Cycle N+1									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2111: y(3)	c(24)	x(-21)	c(25)	x(-22)	2121: y(3)	c(26)	x(-23)	c(27)	x(-24)
2112: y(2)	c(24)	x(-22)	c(25)	x(-23)	2122: y(2)	c(26)	x(-24)	c(27)	x(-25)
2113: y(1)	c(24)	x(-23)	c(25)	x(-24)	2123: y(1)	c(26)	x(-25)	c(27)	x(-26)
2114: y(0)	c(24)	x(-24)	c(25)	x(-25)	2124: y(0)	c(26)	x(-26)	c(27)	x(-27)
Computation Cycle N+2									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2111: y(3)	c(20)	x(-17)	c(21)	x(-18)	2121: y(3)	c(22)	x(-19)	c(23)	x(-20)
2112: y(2)	c(20)	x(-18)	c(21)	x(-19)	2122: y(2)	c(22)	x(-20)	c(23)	x(-21)
2113: y(1)	c(20)	x(-19)	c(21)	x(-20)	2123: y(1)	c(22)	x(-21)	c(23)	x(-22)
2114: y(0)	c(20)	x(-20)	c(21)	x(-21)	2124: y(0)	c(22)	x(-22)	c(23)	x(-23)

FIG. 22

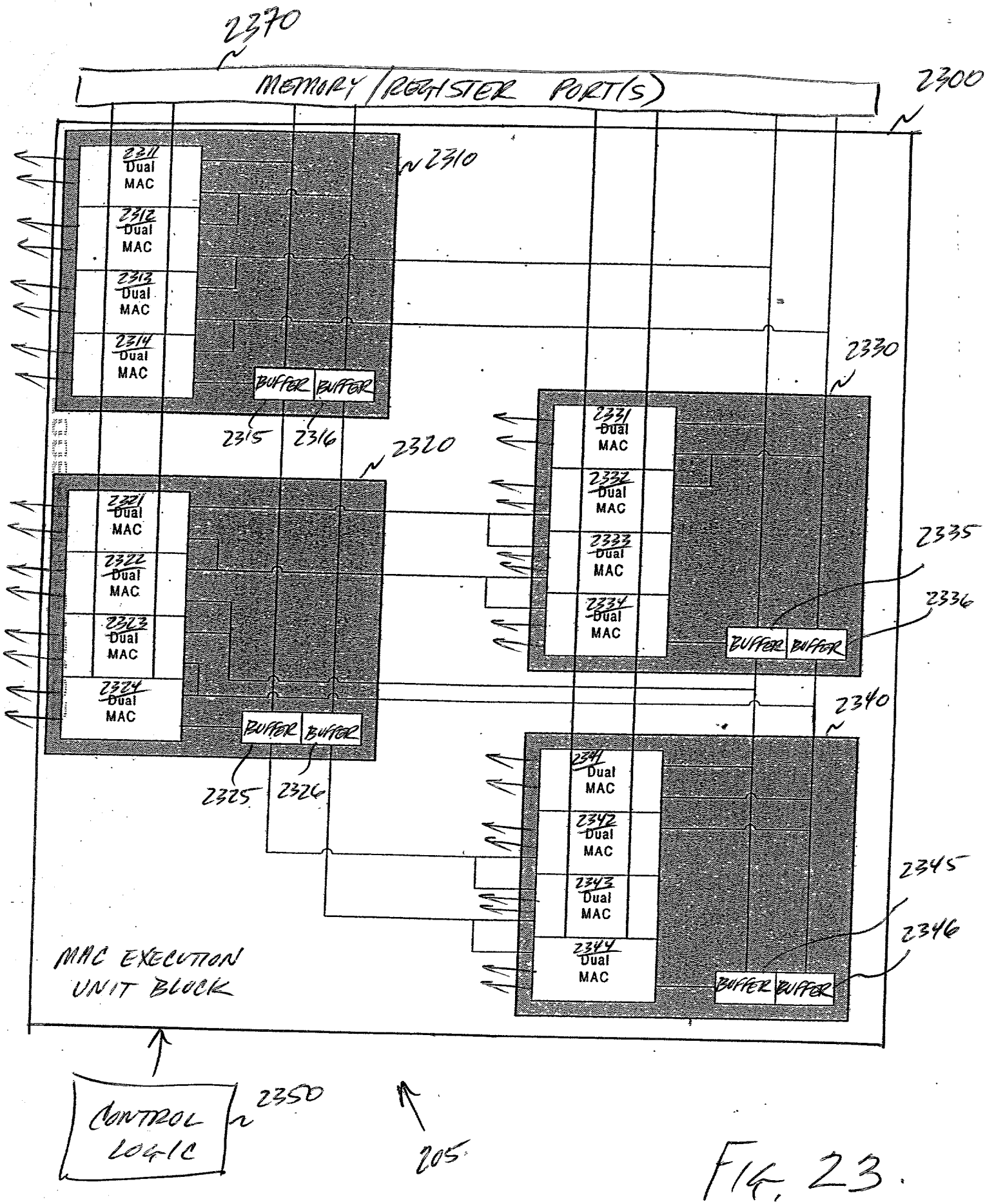
2370
MEMORY / REGISTER PORT(S)
2300
2310
2311 Dual MAC
2312 Dual MAC
2313 Dual MAC
2314 Dual MAC
BUFFER
BUFFER
2315
2316
2320
2321 Dual MAC
2322 Dual MAC
2323 Dual MAC
2324 Dual MAC
BUFFER
BUFFER
2325
2326
2330
2331 Dual MAC
2332 Dual MAC
2333 Dual MAC
2334 Dual MAC
2335
2336
BUFFER
BUFFER
2340
2341 Dual MAC
2342 Dual MAC
2343 Dual MAC
2344 Dual MAC
2345
2346
BUFFER
BUFFER
MAC EXECUTION UNIT BLOCK
CONTROL LOGIC
2350
205

FIG. 23.

2400

Computation Cycle N									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2311: y(7)	c(28)	x(-21)	c(29)	x(-22)	2331: y(7)	c(30)	x(-23)	c(31)	x(-24)
2312: y(6)	c(28)	x(-22)	c(29)	x(-23)	2332: y(6)	c(30)	x(-24)	c(31)	x(-25)
2313: y(5)	c(28)	x(-23)	c(29)	x(-24)	2333: y(5)	c(30)	x(-25)	c(31)	x(-26)
2314: y(4)	c(28)	x(-24)	c(29)	x(-25)	2334: y(4)	c(30)	x(-26)	c(31)	x(-27)
2321: y(3)	c(28)	x(-25)	c(29)	x(-26)	2341: y(3)	c(30)	x(-27)	c(31)	x(-28)
2322: y(2)	c(28)	x(-26)	c(29)	x(-27)	2342: y(2)	c(30)	x(-28)	c(31)	x(-29)
2323: y(1)	c(28)	x(-27)	c(29)	x(-28)	2343: y(1)	c(30)	x(-29)	c(31)	x(-30)
2324: y(0)	c(28)	x(-28)	c(29)	x(-29)	2344: y(0)	c(30)	x(-30)	c(31)	x(-31)
Computation Cycle N+1									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2311: y(7)	c(24)	x(-17)	c(25)	x(-18)	2331: y(7)	c(26)	x(-19)	c(27)	x(-20)
2312: y(6)	c(24)	x(-18)	c(25)	x(-19)	2332: y(6)	c(26)	x(-20)	c(27)	x(-21)
2313: y(5)	c(24)	x(-19)	c(25)	x(-20)	2333: y(5)	c(26)	x(-21)	c(27)	x(-22)
2314: y(4)	c(24)	x(-20)	c(25)	x(-21)	2334: y(4)	c(26)	x(-22)	c(27)	x(-23)
2321: y(3)	c(24)	x(-21)	c(25)	x(-22)	2341: y(3)	c(26)	x(-23)	c(27)	x(-24)
2322: y(2)	c(24)	x(-22)	c(25)	x(-23)	2342: y(2)	c(26)	x(-24)	c(27)	x(-25)
2323: y(1)	c(24)	x(-23)	c(25)	x(-24)	2343: y(1)	c(26)	x(-25)	c(27)	x(-26)
2324: y(0)	c(24)	x(-24)	c(25)	x(-25)	2344: y(0)	c(26)	x(-26)	c(27)	x(-27)
Computation Cycle N+2									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2311: y(7)	c(20)	x(-13)	c(21)	x(-14)	2331: y(7)	c(22)	x(-15)	c(23)	x(-16)
2312: y(6)	c(20)	x(-14)	c(21)	x(-15)	2332: y(6)	c(22)	x(-16)	c(23)	x(-17)
2313: y(5)	c(20)	x(-15)	c(21)	x(-16)	2333: y(5)	c(22)	x(-17)	c(23)	x(-18)
2314: y(4)	c(20)	x(-16)	c(21)	x(-17)	2334: y(4)	c(22)	x(-18)	c(23)	x(-19)
2321: y(3)	c(20)	x(-17)	c(21)	x(-18)	2341: y(3)	c(22)	x(-19)	c(23)	x(-20)
2322: y(2)	c(20)	x(-18)	c(21)	x(-19)	2342: y(2)	c(22)	x(-20)	c(23)	x(-21)
2323: y(1)	c(20)	x(-19)	c(21)	x(-20)	2343: y(1)	c(22)	x(-21)	c(23)	x(-22)
2324: y(0)	c(20)	x(-20)	c(21)	x(-21)	2344: y(0)	c(22)	x(-22)	c(23)	x(-23)

FIG. 24

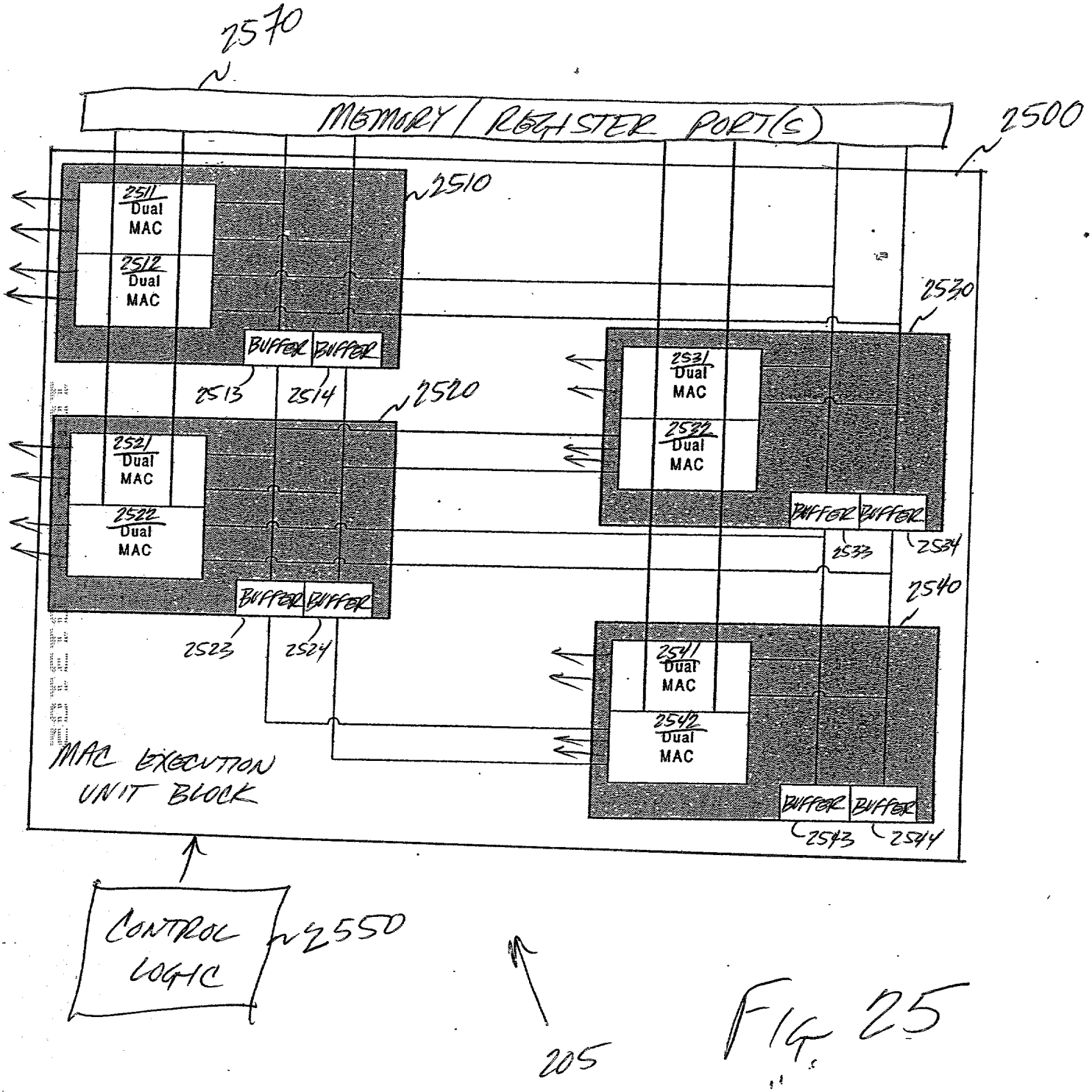
2570
MEMORY / REGISTER PORT(S)
2500
2510
2511 Dual MAC
2512 Dual MAC
BUFFER
BUFFER
2513
2514
2520
2521 Dual MAC
2522 Dual MAC
BUFFER
BUFFER
2523
2524
2530
2531 Dual MAC
2532 Dual MAC
BUFFER
BUFFER
2533
2534
2540
2541 Dual MAC
2542 Dual MAC
BUFFER
BUFFER
2543
2544
MAC EXECUTION UNIT BLOCK
CONTROL LOGIC
2550
205

FIG 25

2600

Computation Cycle N									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2511: y(6)	c(28)	x(-22)	c(29)	x(-23)	2531: y(6)	c(30)	x(-24)	c(31)	x(-25)
2512: y(4)	c(28)	x(-24)	c(29)	x(-25)	2532: y(4)	c(30)	x(-26)	c(31)	x(-27)
2521: y(2)	c(28)	x(-26)	c(29)	x(-27)	2541: y(2)	c(30)	x(-28)	c(31)	x(-29)
2522: y(0)	c(28)	x(-28)	c(29)	x(-29)	2542: y(0)	c(30)	x(-30)	c(31)	x(-31)
Computation Cycle N+1									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2511: y(6)	c(24)	x(-18)	c(25)	x(-19)	2531: y(6)	c(26)	x(-20)	c(27)	x(-21)
2512: y(4)	c(24)	x(-20)	c(25)	x(-21)	2532: y(4)	c(26)	x(-22)	c(27)	x(-23)
2521: y(2)	c(24)	x(-22)	c(25)	x(-23)	2541: y(2)	c(26)	x(-24)	c(27)	x(-25)
2522: y(0)	c(24)	x(-24)	c(25)	x(-25)	2542: y(0)	c(26)	x(-26)	c(27)	x(-27)
Computation Cycle N+2									
MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC	1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2511: y(6)	c(20)	x(-14)	c(21)	x(-15)	2531: y(6)	c(22)	x(-16)	c(23)	x(-17)
2512: y(4)	c(20)	x(-16)	c(21)	x(-17)	2532: y(4)	c(22)	x(-18)	c(23)	x(-19)
2521: y(2)	c(20)	x(-18)	c(21)	x(-19)	2541: y(2)	c(22)	x(-20)	c(23)	x(-21)
2522: y(0)	c(20)	x(-20)	c(21)	x(-21)	2542: y(0)	c(22)	x(-22)	c(23)	x(-23)

FIG. 26

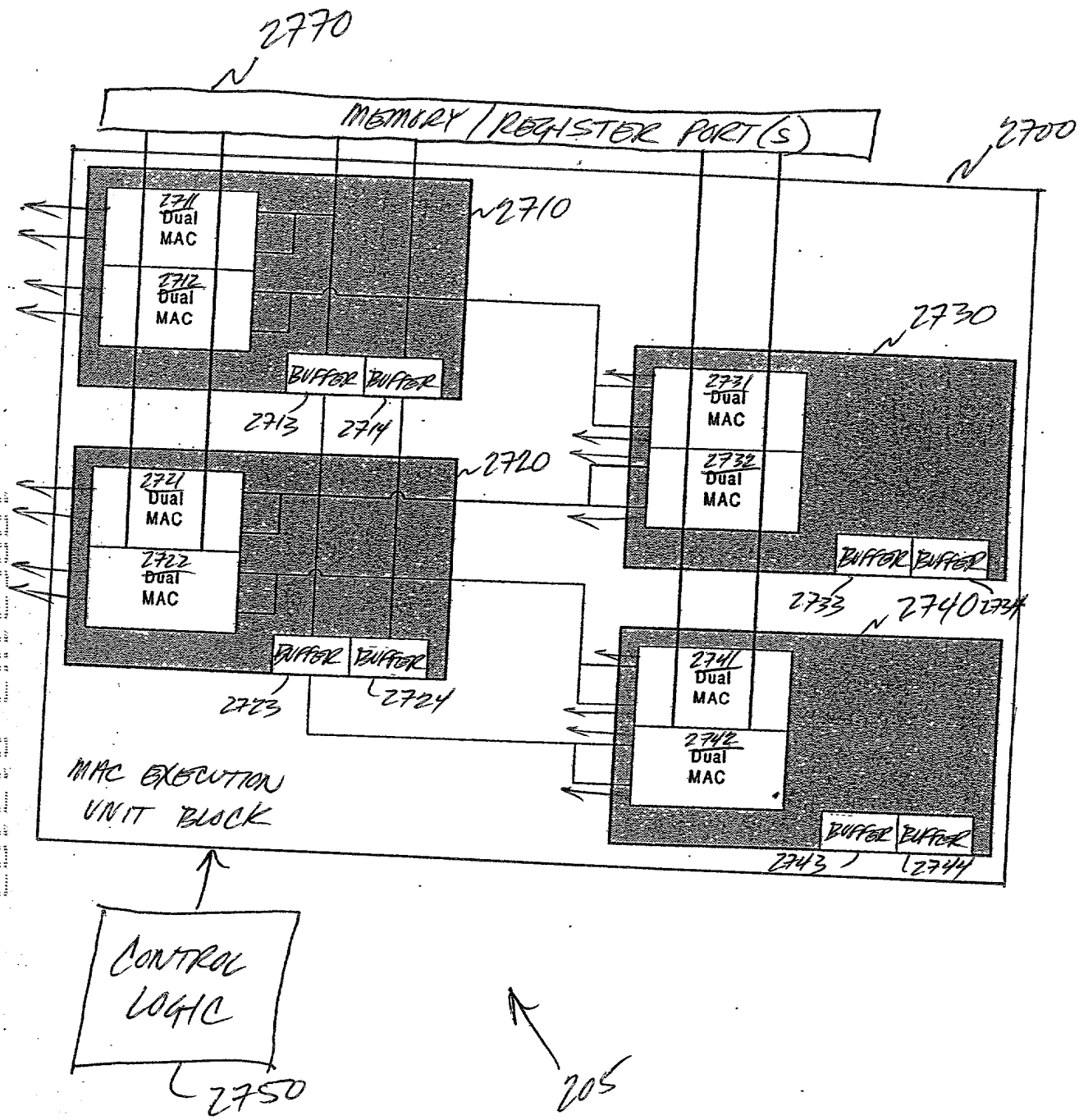
2770
MEMORY / REGISTER PORT(S)
2700
2710
2711 Dual MAC
2712 Dual MAC
BUFFER
BUFFER
2713
2714
2720
2721 Dual MAC
2722 Dual MAC
BUFFER
BUFFER
2723
2724
2730
2731 Dual MAC
2732 Dual MAC
BUFFER
BUFFER
2733
2734
2740
2741 Dual MAC
2742 Dual MAC
BUFFER
BUFFER
2743
2744
MAC EXECUTION UNIT BLOCK
CONTROL LOGIC
2750
205

FIG. 27

2800

Computation Cycle N										
MAC		1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC		1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2711	y(7)			c(29)	x(-19)	2731	y(7)			c(31)	x(-20)
	y(6)	c(28)	x(-19)				y(6)	c(30)	x(-20)		
2712	y(5)			c(29)	x(-20)	2732	y(5)			c(31)	x(-21)
	y(4)	c(28)	x(-20)				y(4)	c(30)	x(-21)		
2721	y(3)			c(29)	x(-21)	2741	y(3)			c(31)	x(-22)
	y(2)	c(28)	x(-21)				y(2)	c(30)	x(-22)		
2722	y(1)			c(29)	x(-22)	2742	y(1)			c(31)	x(-23)
	y(0)	c(28)	x(-22)				y(0)	c(30)	x(-23)		
Computation Cycle N+1										
MAC		1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC		1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2711	y(7)			c(25)	x(-17)	2731	y(7)			c(27)	x(-18)
	y(6)	c(24)	x(-17)				y(6)	c(26)	x(-18)		
2712	y(5)			c(25)	x(-18)	2732	y(5)			c(27)	x(-19)
	y(4)	c(24)	x(-18)				y(4)	c(26)	x(-19)		
2721	y(3)			c(25)	x(-19)	2741	y(3)			c(27)	x(-20)
	y(2)	c(24)	x(-19)				y(2)	c(26)	x(-20)		
2722	y(1)			c(25)	x(-20)	2742	y(1)			c(27)	x(-21)
	y(0)	c(24)	x(-20)				y(0)	c(26)	x(-21)		
Computation Cycle N+2										
MAC		1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input	MAC		1st MAC Input	3rd MAC Input	2nd MAC Input	4th MAC Input
2711	y(7)			c(21)	x(-15)	2731	y(7)			c(23)	x(-16)
	y(6)	c(20)	x(-15)				y(6)	c(22)	x(-16)		
2712	y(5)			c(21)	x(-16)	2732	y(5)			c(23)	x(-17)
	y(4)	c(20)	x(-16)				y(4)	c(22)	x(-17)		
2721	y(3)			c(21)	x(-17)	2741	y(3)			c(23)	x(-18)
	y(2)	c(20)	x(-17)				y(2)	c(22)	x(-18)		
2722	y(1)			c(21)	x(-18)	2742	y(1)			c(23)	x(-19)
	y(0)	c(20)	x(-18)				y(0)	c(22)	x(-19)		

Fig. 28